said contact layer is formed such that said contact layer is buried in said first epitaxially grown layer to reach said capacitor node layer; and

the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

8. (Amended) The semiconductor memory device according to claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node layer, and the other of said source/drain diffusion layers is connected to said contact layer through a buried diffusion layer formed in an upper side portion of said contact layer.

9. (Amended) The semiconductor memory device according to claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node, and the other of said source/drain diffusion layers is connected to a top surface of said contact layer through a connection conductor formed on a surface thereof.

G3 cont.

10. (Amended) The semiconductor memory device according to claim 2, wherein:

said semiconductor layer comprises a bulk semiconductor layer of another semiconductor substrate bonded to said semiconductor substrate in which said capacitors are formed, and an epitaxially grown layer formed on said bulk semiconductor layer;

said contact layer is formed such that said contact layer is buried in said bulk semiconductor layer to reach said capacitor node layer; and

the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

G4 Sub B

12. (Amended) A semiconductor device comprising:

a semiconductor substrate;